PD - 97074A

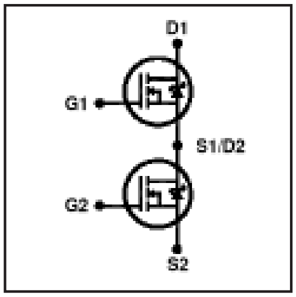
International
IOR Rectifier

IRFI4019H-117P

DIGITAL AUDIO MOSFET

Features
- Integrated Half-Bridge Package
- Reduces the Part Count by Half
- Facilitates Better PCB Layout
- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low $R_{DS(ON)}$ for Improved Efficiency
- Low Qg and Qsw for Better THD and Improved Efficiency
- Low Qrr for Better THD and Lower EMI
- Can Delivery up to 200W per Channel into 8Ω Load in Half-Bridge Configuration Amplifier
- Lead-Free Package

Key Parameters ⑥		
V_{DS}	150	V
$R_{DS(ON)}$ typ. @ 10V	80	mΩ
Q_g typ.	13	nC
Q_{sw} typ.	4.1	nC
$R_{G(int)}$ typ.	2.5	Ω
T_J max	150	°C



TO-220 Full-Pak 5 PIN

G1, G2	D1, D2	S1, S2
Gate	Drain	Source

Description

This Digital Audio MosFET Half-Bridge is specifically designed for Class D audio amplifier applications. It consists of two power MosFET switches connected in half-bridge configuration. The latest process is used to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery, and internal Gate resistance are optimized to improve key Class D audio amplifier performance factors such as efficiency, THD and EMI. These combine to make this Half-Bridge a highly efficient, robust and reliable device for Class D audio amplifier applications.

Absolute Maximum Ratings ⑥

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	150	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	8.7	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	6.2	
I_{DM}	Pulsed Drain Current ①	34	
E_{AS}	Single Pulse Avalanche Energy②	77	mJ
P_D @T_C = 25°C	Power Dissipation ④	18	W
P_D @T_C = 100°C	Power Dissipation ④	7.2	
	Linear Derating Factor	0.15	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

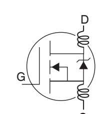
Thermal Resistance ⑥

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	6.9	
$R_{\theta JA}$	Junction-to-Ambient ④	—	65	

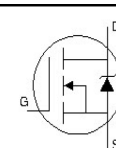
Notes ① through ⑥ are on page 2

8/22/06

Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified) ⑥

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	150	——	——	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.19	——	V/°C	Reference to 25°C, $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	80	95	mΩ	$V_{GS} = 10V$, $I_D = 5.2A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	4.9	V	$V_{DS} = V_{GS}$, $I_D = 50\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	——	-11	——	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	$V_{DS} = 150V$, $V_{GS} = 0V$
		——	——	250		$V_{DS} = 150V$, $V_{GS} = 0V$, $T_J = 125°C$
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	——	——	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	11	——	——	S	$V_{DS} = 50V$, $I_D = 5.2A$
Q_g	Total Gate Charge	——	13	20		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	——	3.3	——		$V_{DS} = 75V$
Q_{gs2}	Post-Vth Gate-to-Source Charge	——	0.8	——	nC	$V_{GS} = 10V$
Q_{gd}	Gate-to-Drain Charge	——	3.9	——		$I_D = 5.2A$
Q_{godr}	Gate Charge Overdrive	——	5.0	——		See Fig. 6 and 19
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	——	4.1	——		
$R_{G(int)}$	Internal Gate Resistance	——	2.5	——	Ω	
$t_{d(on)}$	Turn-On Delay Time	——	7.0	——		$V_{DD} = 75V$, $V_{GS} = 10V$ ③
t_r	Rise Time	——	6.6	——		$I_D = 5.2A$
$t_{d(off)}$	Turn-Off Delay Time	——	13	——	ns	$R_G = 2.4\Omega$
t_f	Fall Time	——	3.1	——		
C_{iss}	Input Capacitance	——	810	——		$V_{GS} = 0V$
C_{oss}	Output Capacitance	——	100	——	pF	$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	——	15	——		$f = 1.0MHz$, See Fig.5
C_{oss}	Effective Output Capacitance	——	97	——		$V_{GS} = 0V$, $V_{DS} = 0V$ to 120V
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	——	7.5	——		from package and center of die contact

Diode Characteristics ⑥

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S @ $T_C = 25°C$	Continuous Source Current (Body Diode)	——	——	8.7	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	34		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	——	——	1.3	V	$T_J = 25°C$, $I_S = 5.2A$, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	——	57	86	ns	$T_J = 25°C$, $I_F = 5.2A$
Q_{rr}	Reverse Recovery Charge	——	140	210	nC	di/dt = 100A/μs ③

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting $T_J = 25°C$, L = 5.8mH, $R_G = 25\Omega$, $I_{AS} = 5.2A$.
③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
④ R_θ is measured at T_J of approximately 90°C.
⑤ Limited by Tjmax. See Figs. 14, 15, 17a, 17b for repetitive avalanche information
⑥ Specifications refer to single MosFET.

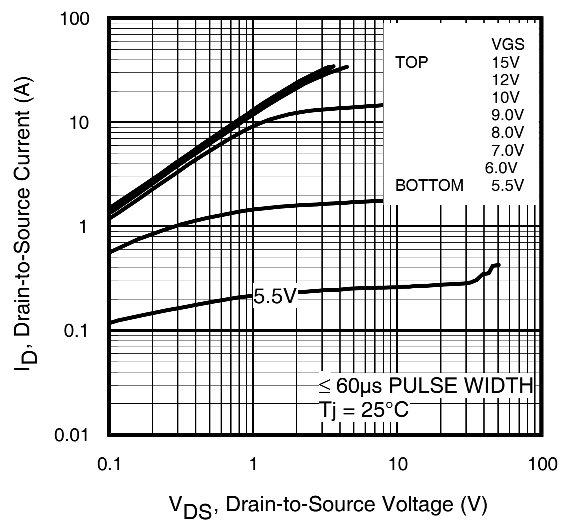


Fig 1. Typical Output Characteristics

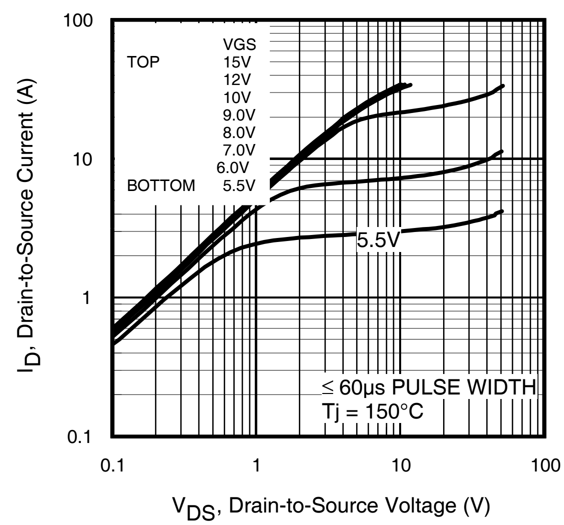


Fig 2. Typical Output Characteristics

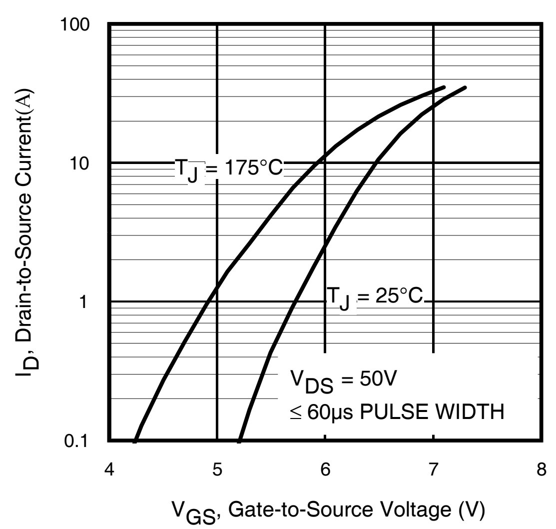


Fig 3. Typical Transfer Characteristics

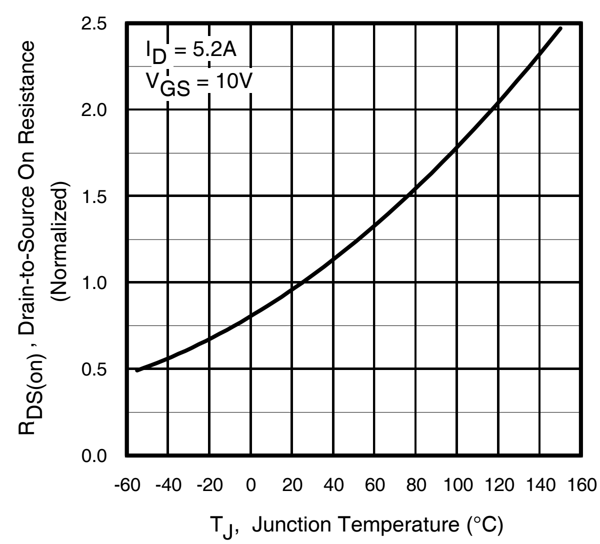


Fig 4. Normalized On-Resistance vs. Temperature

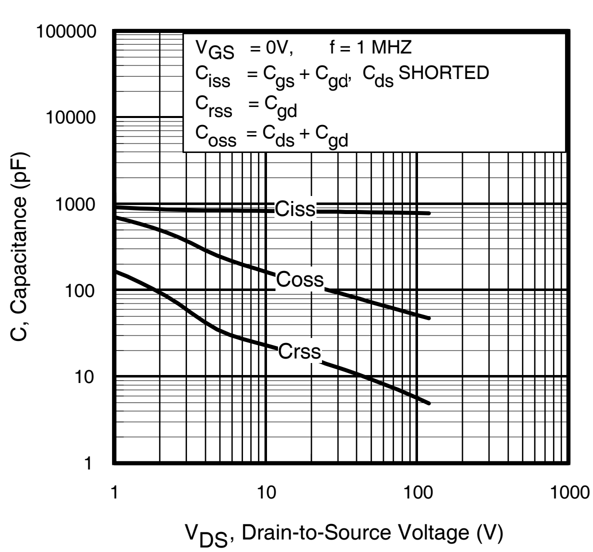


Fig 5. Typical Capacitance vs.Drain-to-Source Voltage

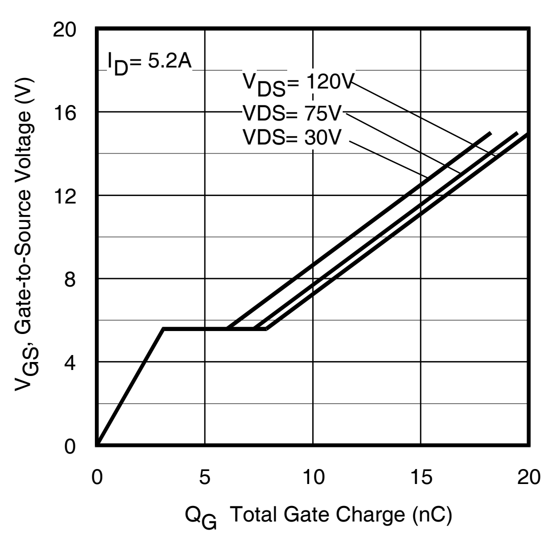


Fig 6. Typical Gate Charge vs.Gate-to-Source Voltage

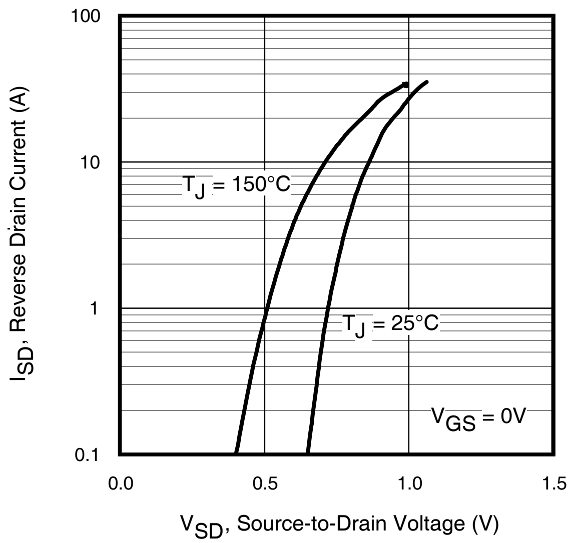


Fig 7. Typical Source-Drain Diode Forward Voltage

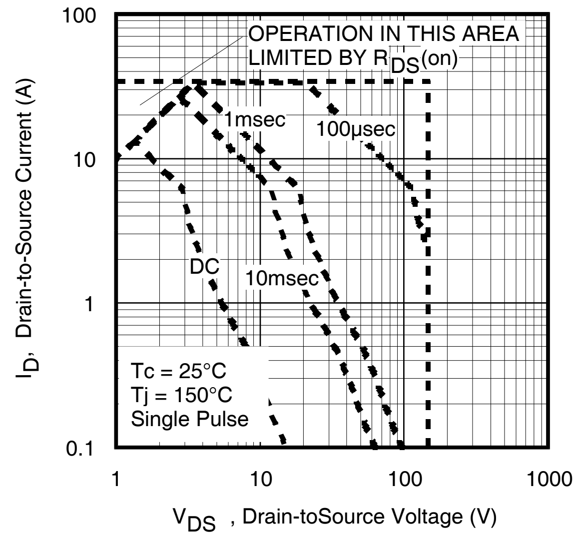


Fig 8. Maximum Safe Operating Area

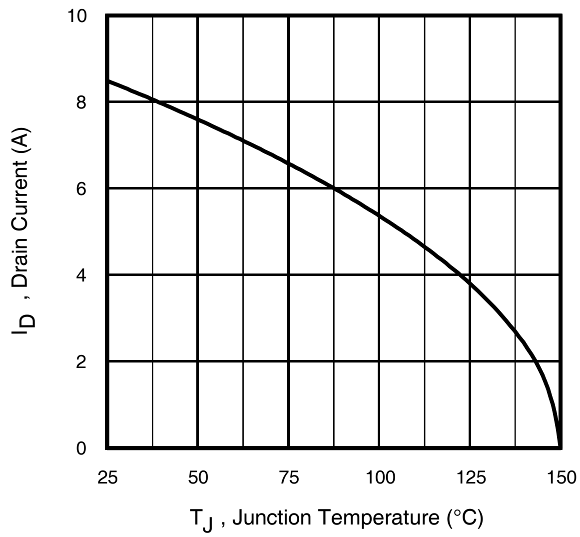


Fig 9. Maximum Drain Current vs. Case Temperature

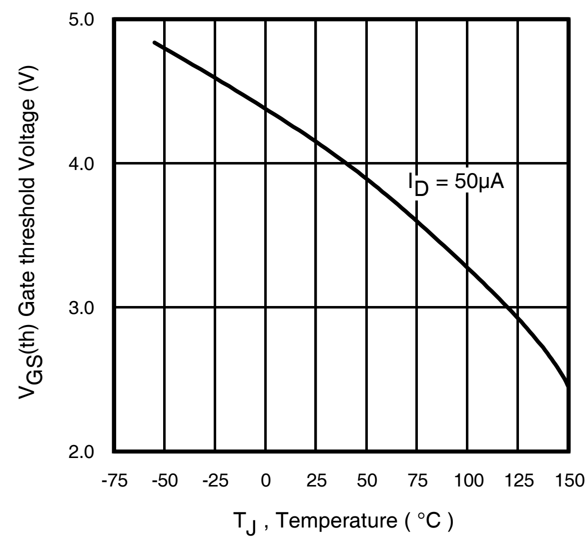
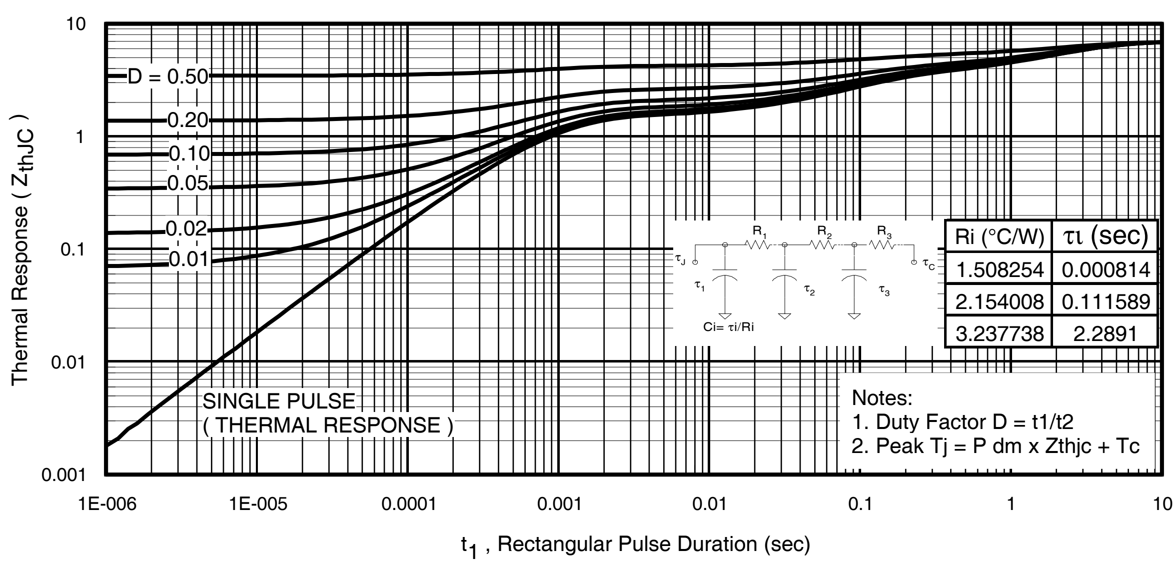


Fig 10. Threshold Voltage vs. Temperature



Ri (°C/W)	τi (sec)
1.508254	0.000814
2.154008	0.111589
3.237738	2.2891

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

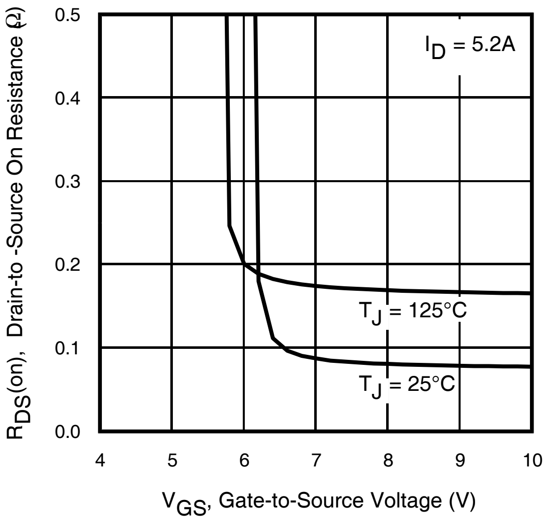


Fig 12. On-Resistance Vs. Gate Voltage

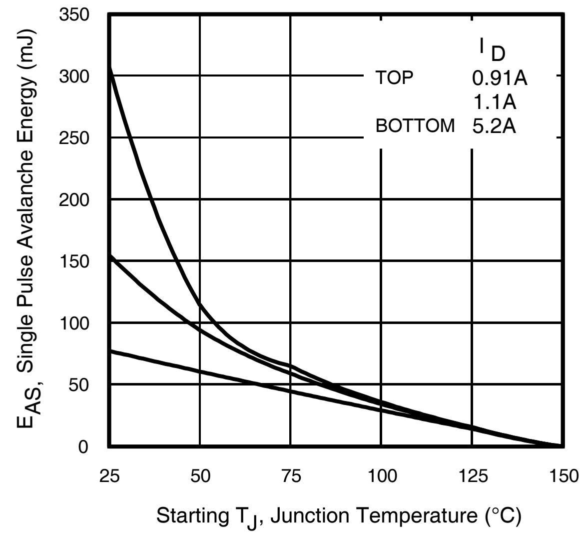
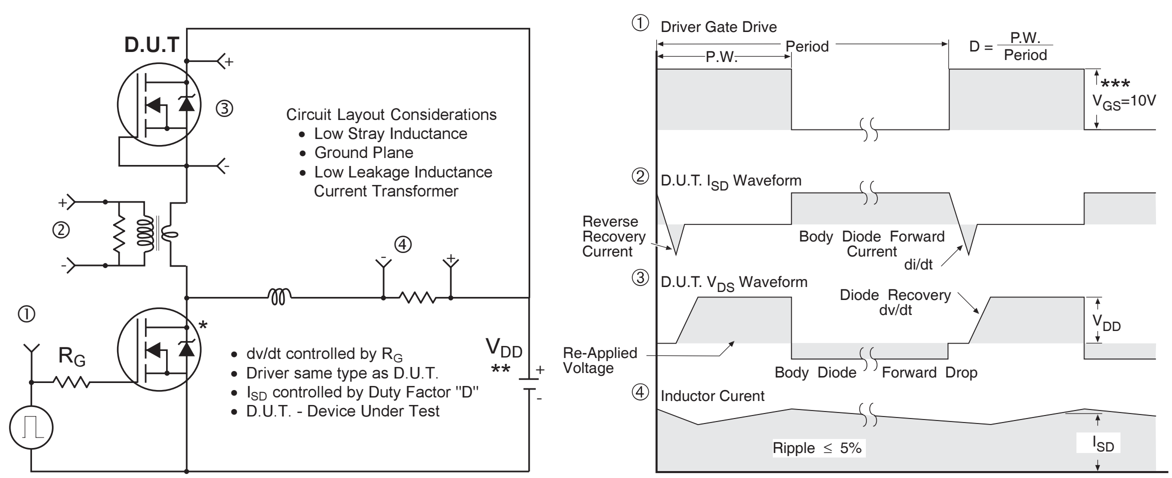


Fig 13. Maximum Avalanche Energy Vs. Drain Current



* Use P-Channel Driver for P-Channel Measurements
** Reverse Polarity for P-Channel

*** V_{GS} = 5V for Logic Level Devices

Fig 14. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

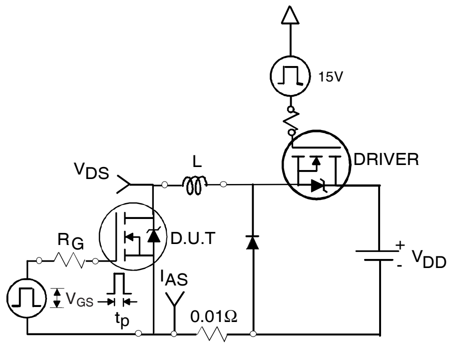


Fig 15a. Unclamped Inductive Test Circuit

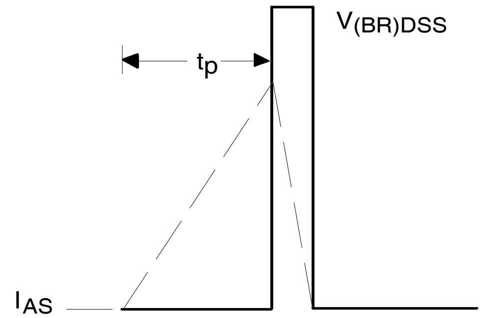


Fig 15b. Unclamped Inductive Waveforms

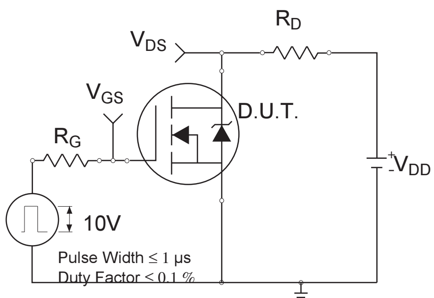


Fig 16a. Switching Time Test Circuit

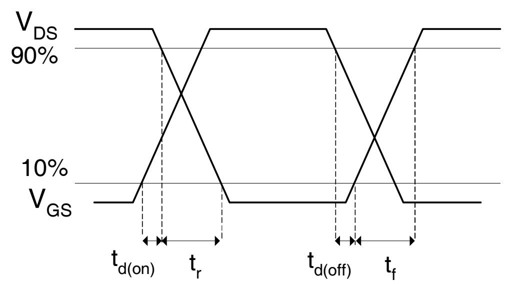


Fig 16b. Switching Time Waveforms

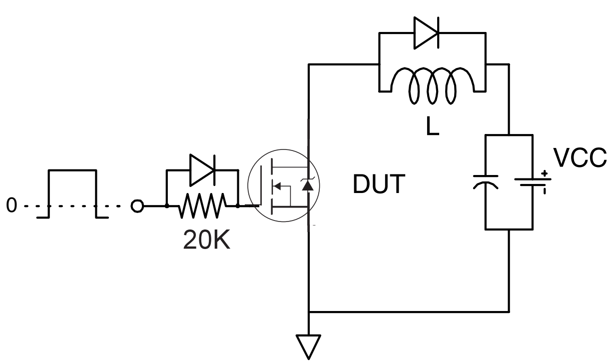


Fig 17a. Gate Charge Test Circuit

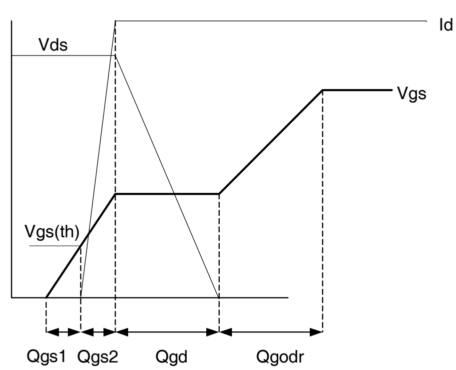
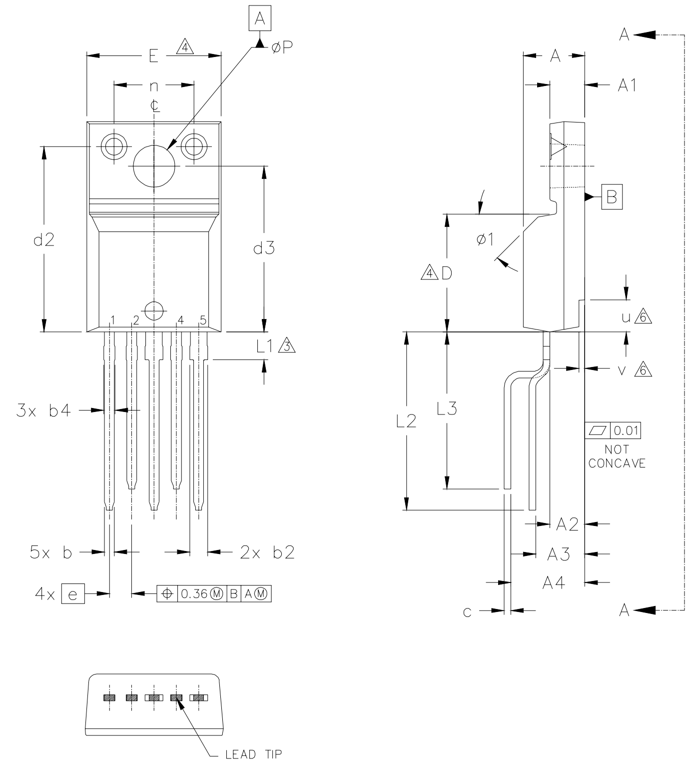


Fig 17b Gate Charge Waveform

TO-220 Full-Pak 5-Pin Package Outline, Lead-Form Option 117

(Dimensions are shown in millimeters (inches))



NOTES:

1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	
A1	2.57	2.83	.101	.111	
A2	2.51	2.85	.099	.112	
A3	3.73	4.24	.147	.167	
A4	5.79	6.29	.228	.248	
b	0.61	0.95	0.24	.037	
b1	0.56	0.90	.022	0.35	5
b2	1.13	1.48	0.44	.058	
b3	1.08	1.43	0.42	.056	5
b4	0.76	1.06	.030	.042	
b5	0.71	1.01	.028	.040	5
c	0.33	0.63	.013	.025	
c1	0.28	0.58	.011	.023	5
D	8.65	9.80	.341	.386	4
d1	15.80	16.12	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.30	12.92	.484	.509	
E	9.63	10.63	.379	.419	4

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
e	1.70 BSC		.067 BSC		
L	13.20	13.73	.520	.541	
L1	1.91	2.31	.075	.091	3
L2	12.7	13.46	.500	.530	
L3	10.92	11.68	.430	.460	
n	6.05	6.15	.238	.242	
øP	3.05	3.45	.120	.136	
u	2.40	2.50	.094	.098	6
v	0.40	0.50	.016	.020	6
ø1	–	45°	–	45°	

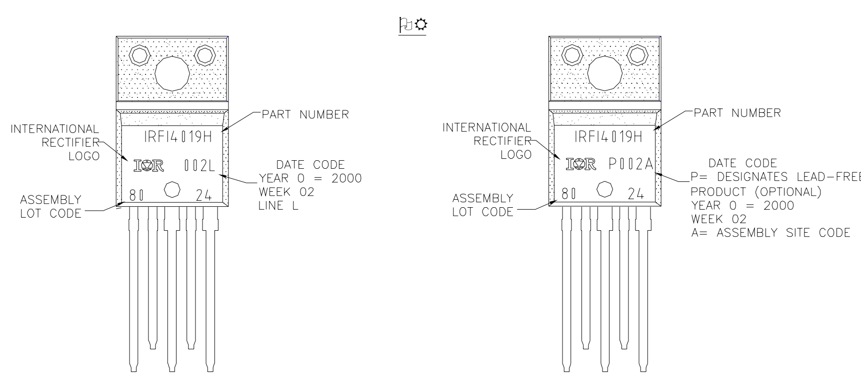
LEAD ASSIGNMENTS

1 - SOURCE 2
2 - GATE 2
3 - DRAIN 2 / SOURCE 1
4 - GATE 1
5 - DRAIN 1

TO-220 Full-Pak 5-Pin Part Marking Information

EXAMPLE: THIS IS AN IRFI4019H WITH LOT CODE 8024 ASSEMBLED ON WW02,2000 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead Free"



TO-220AB Full-Pak 5-Pin package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/